REMARKS

The above-referenced patent application has been reviewed in light of the Office Action, mailed November 13, 2002, in which: claims 27-43 are rejected under 35 U.S.C. § 103 as being unpatentable over Sato (US-4,611,236) in light of Tran et al. (US-5,780,883) (hereinafter "Tran"). Reconsideration of the above-referenced patent application in view of the following remarks is respectfully requested.

Multiple informalities and minor omissions are noted in the specification. These minor errors and omissions were made inadvertently and without deceptive intent. Appropriate corrections have been made by the foregoing amendments. It is respectfully requested that Examiner approve and enter these minor corrections. These changes do not limit the scope of the claims or result in prosecution history estoppel.

Claims 27-43 are pending in the application. Claims 27, 30, 31, 38, 40, 41, 42 and 43 have been amended. Claims 40-43 have been broadened. Claims 44-47 are new. Claims 1-26 have been cancelled because they are being prosecuted in the parent application. No prosecution history estoppel results from the cancellation because it merely permits those claims to be prosecuted separately. No claimed subject matter of any kind has been surrendered by these actions. It is respectfully requested that Examiner approve and enter these changes.

I. Claims 27-43

(a)

Examiner has rejected claims 27-43. However, in a previous Office Action in the parent application Examiner previously **allowed** these **same** claims in the presence of the same Sato and

Tran patents. See Office Action dated March 7, 2001, in application 09/262,458, titled "Gate Array Architecture," by Possley, filed March 4, 1999, assigned to the assignee of the present invention. After Examiner allowed these claims in the parent application 09/262,458, Applicant filed this continuation to permit these allowed claims to proceed to issuance. Applicant respectfully submits that Examiner's previous allowance of these claims was correct and that these claims distinguish over the cited patents, and therefore requests Examiner withdraw his rejection.

(b)

Examiner has rejected claims 27-43 under 35 U.S.C. § 103 as being unpatentable over Sato in light of Tran, stating that "it would have been obvious to one of ordinary skill in the art to use polysilicon landing sites in Sato on both N-type and P-type transistors to form a basic cell as taught by Tran et al." The rejection of these claims on this basis is respectfully traversed. Applicant respectfully asserts that Examiner has failed to establish a *prima facie* case of obviousness under section 103 and, therefore, claims 27-43 are in a condition for allowance.

Section 2143 of the Manual of Patent Examining Procedure (hereinafter "MPEP") sets forth the requirements Examiner must satisfy to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Section 2143 requires the cited patents to contain a suggestion or motivation to combine them. Examiner has failed to make this showing because Examiner does not point out a suggestion or motivation to combine. Instead, Examiner only makes a conclusory statement that "it would have been obvious to one of ordinary skill in the art" to combine Sato and Tran. In so doing, Examiner has engaged in hindsight speculation that section 2143 and the Federal Circuit expressly proscribe: "the level of skill in the art cannot be relied upon to provide the suggestion to combine references," (MPEP § 2143, citing *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308 (Fed. Cir. 1999)). Furthermore, Examiner has failed to offer any findings, support or explanation for Examiner's conclusory assertion that "it would have been obvious to one of ordinary skill in the

art." Examiner thereby commits errors that section 2143 forbids. Section 2143 highlights these errors, citing *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) ("there was no finding 'as to the specific understanding or principle within the knowledge of the skilled artisan' that would have provided the motivation") and *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988) (where "the examiner and Board asserted that it would have been within the skill of the art . . . the court found there was no support or explanation of this conclusion and reversed").

It is noteworthy that section 2143 takes pains to make this point clear, elaborating that "a statement that modifications of the prior art to meet the claimed invention would have been 'well within the ordinary skill of the art at the time the claimed invention was made' because the references relied upon teach that all aspects of the claimed invention were individually known in the art is **not sufficient** to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993) (emphasis added). By repeating the mistakes criticized in section 2143 and failing to show a suggestion or motivation to combine Sato and Tran, Examiner has thereby failed to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

Not only does Examiner fail to show a motivation or suggestion to combine the Sato and Tran patents, but also both patents actually teach away from Applicant's invention. Since each patent teaches away, one of ordinary skill in the art would not try to combine them. Neither is suitable for low power, high density logic devices comprising a multitude of flip-flops. Sato is not directed to low power, high density logic devices because in Sato, the large center array (denoted BLL in Figure 6(a) of Sato), is meant for high power. Sato describes this array as "having a relatively larger size and higher power capacity" (Sato, column 3, line 65). Thus, Sato teaches away from low power, high density logic devices.

Likewise, Tran is not directed to low power, high density logic devices either. In Tran, the alternating diffusion regions require significant space between them. As is well known in the art, P-diffusion strips must be surrounded by N-well regions. Thus, the alternating P- and N- diffusion strips shown in Figure 3A of Tran require one N-well for each P-diffusion region, i.e. a single N-well region cannot surround more than one P-diffusion region. Furthermore, Tran contemplates using the inner diffusion strips, labeled 44 and 46 in figure 3A of Tran, as transmission gates and not as logic gates (see Tran, column 4, lines 61-65). Thus Tran also teaches away from low power, high density logic devices.

Since both the Sato and Tran patents teach away from the rejected claims, Applicant submits that there is no motivation to combine them and, therefore, they cannot be combined under 35 U.S.C. § 103 and MPEP § 2143. Thus, Applicant respectfully traverses Examiner's rejection of claims 27-43 under 35 U.S.C. § 103.

Even if one were to assume a motivation to combine the Sato and Tran patents cited by the Examiner, which Applicant disputes, the Examiner has nonetheless failed to make a *prima facie* case of obviousness under 35 U.S.C. § 103 because Examiner's proposed combination does not have a reasonable expectation of success. Section 2142 of the MPEP requires that a proposed combination of patents have a reasonable expectation of success in order to state a *prima facie* case of obviousness under 35 U.S.C. § 103. Examiner's proposed combination of Sato and Tran does not have a reasonable expectation of success because it would be unworkable. Since the large N- and P-diffusion regions of Sato (denoted BCL in Sato, Figures 6(a) & 9) would form high-power transistors, the proposed combination would be detrimental to the operation of a low power, high density device. Furthermore, one cannot simply shrink the features of Sato in order to obtain normal-power BCL transistors because shrinking the BCL transistors would shrink the regions

required for routing (denoted S1 and S2 in Sato, Figure 9), thereby making routing in S1 and S2 impossible.

It is apparent that Examiner's proposed combination would not be successful for its intended purpose as required by MPEP section 2142 because, for example, implementing flip-flops would consume excessive amounts of power and exhibit high capacitance, as demonstrated. Examiner has therefore failed to make a *prima facie* case of obviousness under 35 U.S.C. § 103. Thus, Applicant traverses Examiner's rejection and respectfully asserts that claims 27-43 are in a condition for allowance.

II. Claims 27 and 38

Applicant has amended claim 27 to further clarify and distinguish it from the cited patents. As discussed above, Applicant respectfully asserts that this claim was in condition for allowance without this amendment and, as such, respectfully reserves the right to pursue the original claim language on any subsequent appeal. Applicant has similarly amended claim 38 but again reserves the right to pursue the original claim language on any subsequent appeal.

Claim 27 now specifically recites:

> An integrated circuit comprising: a gate array architecture;
> said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least one forming both N-type and P-type transistors;
> wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P- type transistors;
> the relatively sized P-type ~~diffusions~~ diffusion regions being substantially adjacent;
> successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions; ~~and~~
> immediately successive rows within similarly-sized diffusion regions have opposite polarity; **and**

wherein said transistors are formed in said gate array architectur o that an interconnect disposed thereon is capable of connecting said small r tran istors to form internal clock buffers.

Applicant respectfully asserts that this amendment further distinguishes from the cited patents in at least the respect that Sato uses larger transistors to form inverters and Tran teaches that larger transistors are used for inverters and logic gates. Therefore, it is respectfully requested that the Examiner withdraw the rejections to claim 27 and claims 28-37, which depend therefrom.

Claim 38 has been amended in a similar fashion to claim 27 and contains similar limitations to those discussed above with respect to claim 27. Therefore, it is respectfully asserted that claim 38, as currently amended, patentably distinguishes from the cited patents for similar reasons to those discussed with respect to claim 27, above. As such, Applicant respectfully requests that Examiner withdraw the rejections to claim 38 and claims 39-43, which depend therefrom.

III. Claims 44-47

Applicant has added claims 44-47. Applicant respectfully asserts that there is adequate support in the specification for these claims. Such support may be found, for example, in the paragraph beginning at line 3 on page 6, the paragraph beginning at line 21 on page 7, and in FIG. 5. Claims 44 and 45 depend from and include all the limitations of claim 32. Claims 46 and 47 depend from and include all the limitations of claim 43. Therefore, it is respectfully asserted that these claims are patentable on the same basis as those claims, and that these claims patentably distinguish from the cited patents for at least the reasons discussed above with respect to those claims.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 712-1565 or Howard Skaist at (503) 264-0967. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

Jay Beale
Patent Agent
Reg. No. 50,901

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c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

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Angie C. Farr
Name of Person Mailing Correspondence

Angie C. Farr 4/14/03
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